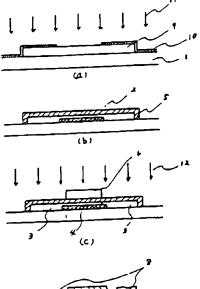
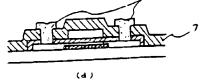
- 1 Insulating Substrate
- 2. Ion Implanted Insulating Layer
- 3. Source Region / Drain Region
- 4. Channel Region

- FROM SEMICONDUCTOR ENERGY LAB

- 5. Gate Insulating Layer
- 6. Gate Electrode
- 7- Interlayer Insulating Layer
- 8. Source Electrode / Drain Region
- 9. Non-Single Crystal Silicon Layer
- 10. Resist Layer
- 11. Oxygen Ion Beam on Nitrogen Ion Beam
- 12. Impunity Ion Beam
- 13. Mask Insulating Layer
- A: Source / Channel Boundary on Drain / channel Boundary





F1G.3

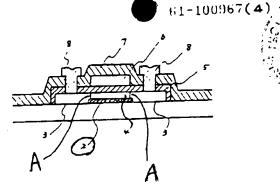


FIG. 7

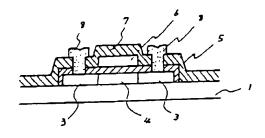
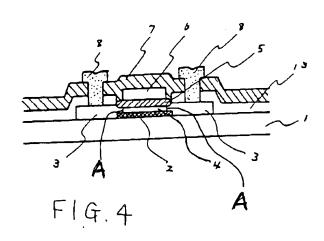


FIG. 2 (PRIOR ART)



Appendix I